DMS LAB Limited

70V BiCDMOS process specification

Description

- 70V 3.0um BiCDMOS process is DMS Lab Limited BCD smart power technologies.
- Main target applications are analog switch ICs, DC-DC converters, driver ICs for capacitive, inductive and resistive loads for applications using 70V supply. The typical breakdown voltage of the power vertical DMOS devices more than 70V.
- The process combines VDMOS and LDMOS, CMOS for different supply application with core bipolar, logic CMOS processing steps to provide a wide variety of MOS and bipolar devices with different voltage levels on the same die.
- The 18 layers core process module is available for 70V breakdown voltage of the VDMOS. This process provides locos insulation, one level poly, and two metal levels.

  With this core module an optimized n-channel vertical and lateral DMOS transistor, logic CMOS and some bipolar transistors can be made.

	Wafer	
1	**N+buried**	
2	**P+buried**	
	Epi	
3	**Well**	
4	**Sinker**	
5	**Division**	
6	**Active**	
7	**P-guard**	
8	**Deep Drain**	
9	**Ch.adjust**	
10	**Gate**	
11	**P-body**	
12	**P+Drain**	
13	**N+Drain**	
14	**Contact**	
15	**Metal 1**	
16	**Via**	
17	**Metal 2**	
18	**Pad**	

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> Key Features

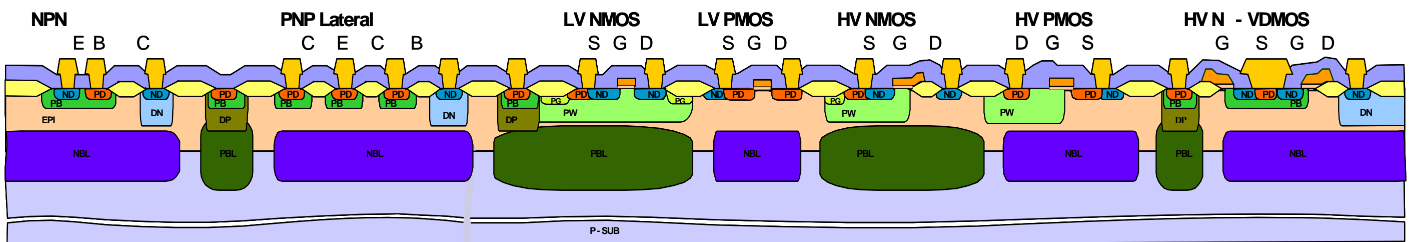
The power vertical NDMOS transistor with low Rdson and small area is the main HV component of the BiCDMOS 70V technology.

3.5um one poly, double metal, one Well BCD process.

A high number of different devices are available:

- 70V n-channel vertical DMOS transistor
- 70V n-channel lateral DMOS transistor;
- 70V p-channel MOS transistor;
- 12V n-channel MOS transistor;
- 12V p-channel MOS transistor;
- 25V NPN transistors;
- 25V PNP transistors;
- Zener diodes;
- Gate oxide capacitors;
- Low resistivity poly-Si resistors;
- Resistors in active layers.

> Schematic cross section



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> Basic design rules

Layer	Min width (um)	Min spacing (um)
Active Area (CMOS)	4.0	2.0
CMOS Gate	3.5	2.0
DMOS Gate	8.0	--
Contact	2.0	2.0
Metal-1	4.0	2.0
VIA	3.0	3.0
Metal-2	5.0	3.0

〉 Device Parameters of main elements for 70V process

ELEMENT	PARAMETER	SPEC		MEASUREMENT CONDITIONS
	UNIT	MIN	MAX	
HV VNDMOS L=8.0 um, W=40 um	VTH, V	1.7	2.3	Id=0.1uA
	IDS, mA	8.0	-	Ug=Ud=5 V
	BVDS, V	70	-	Id=10uA
	Rsp, mOhm*mm2	-	100	Ug=10 V
	IDS, uA	-	50	Ug=Ub=Us=0 V, Ud =50 V
HV LDNMOS L=4 um, W=40 um	VTH, V	1.7	2.3	Id=0.1uA
	IDS, mA	1.5	-	Ug=Ud=10 V
	BVDS, V	70	-	Id=10uA
HV PMOS L=10 um, W=50 um	VTH, V	1.0	1.6	Id=0.1uA
	IDS, mA	0.5	-	Ug=Ud=10 V
	BVDS, V	70	-	Id=10uA
LV NMOS L=3.5 um, W=50 um	VTH, V	0.9	1.3	Id=0.1uA
	IDS, mA	1	3	Ug=Ud=5 V
	BVDS, V	12.0	-	Id=10uA
LV PMOS L=3.5 um, W=50 um	VTH, V	1.3	1.7	Id=0.1uA
	IDS, mA	0.5	2	Ug=Ud=5 V
	BVDS, V	12		Id=10uA
LV NPN Se=10x10 um2	BETA	50	150	Ib=10uA, Uc=1 V
	BVCE0, V	25	-	Ic=10uA, floating base
LV Lateral PNP Wb=4um	BETA	25	-	Ib=-10uA, Uc=-1 V
	BVCE0, V	25	-	Ic=-10uA, floating base
Diode	BV, V	9	-	Id=10uA
Zener Diode	BV, V	5.5	6.5	Id=10uA
Base Resistor	RS, Ohm/sq	550	650	Ir=10uA
PolySi- gate oxide – Well capacitor	Ccs, pF/um2	4,0E-4	5.0E-4	F=1MHz, Vmea=5V